



H61H2-M12

Rev : 1.0

ECS CONFIDENTIAL

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NOTE:
Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev_0_8.pdf,
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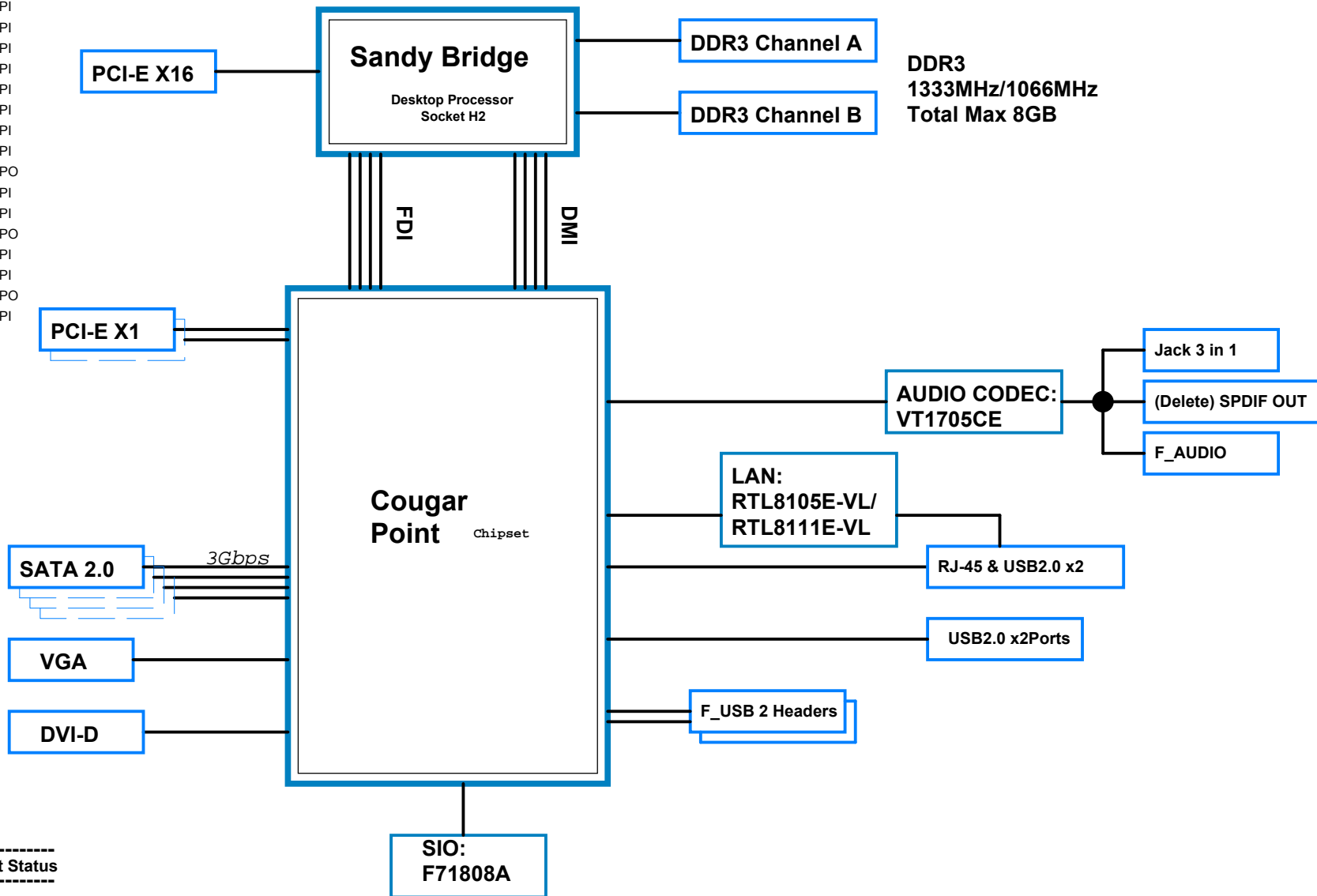
REVISION HISTORY:

Rev	Date	Notes
P61G V1.0	2011/04/07	RED_PCB P/N : 15-Y97-011001 (GE1) / 15-Y97-011000 (CHUANYI) BOM P/N : 81-605-Y97100 EC35 change to EC-cap 1000U-6.3DL EC1, EC4 from 100uF change to 220uF Del RT1, RT3, R137, R180 (Not need compensation of temperature). For 5VSB Inrush Current : R102 from 100k change to 33k. Select TACH0_GPIO17 to decide COM .
H61H2-M12 VA	2011/05/04	Black_PCB P/N : 15-EC7-010010 BOM P/N : 81-605-EC7000/81-605-EC7001(10/100 ; GiGA) PCB Size change to 225*170 mm Del DVI Vcore 減少一相 VIN 電容減少一顆 LAN change to Atheros 8152/8151/8161 Codec change to VT1705CE. USB Power use fuse & Jumper.
H61H2-M12 V1.0	2011/07/12	Black_PCB P/N : 15-EC7-011000/15-EC7-011001 BOM P/N : PCB Size change to 225*170 mm

RD : Jayson
LAYOUT :
EMI :

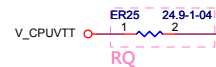
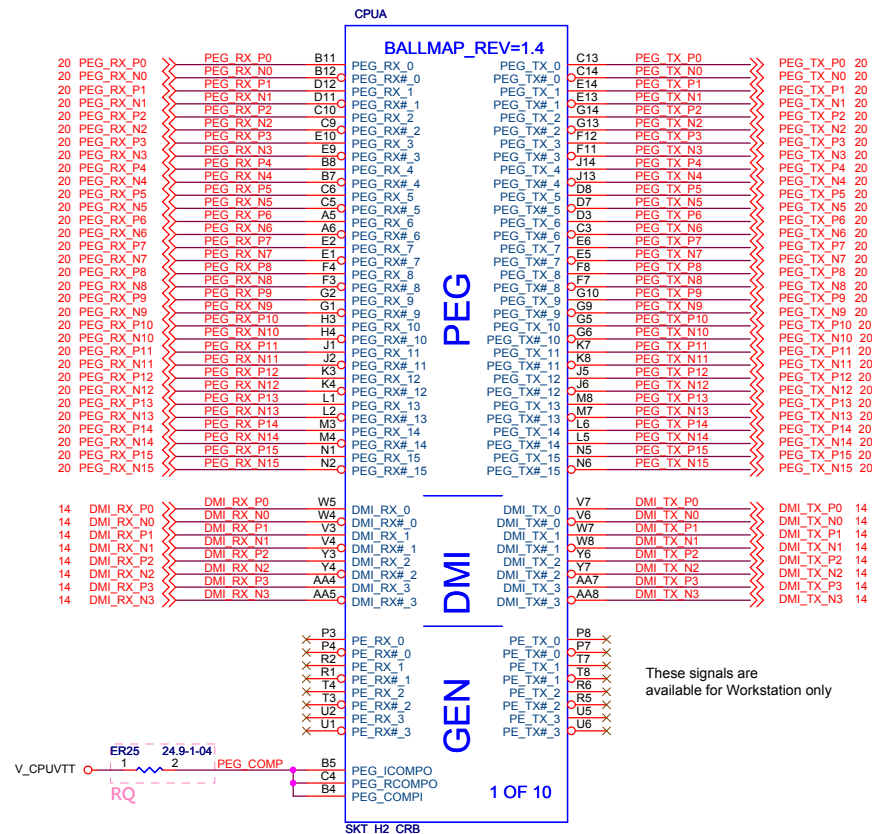
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI
GPIO15	3VSB	Down Voltage for DIMM	GPO
GPIO48	VCC3	Down Voltage for DIMM	GPI



SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
PIN23	5VSB	Power LED	GPIO25/LEDVCC/WDTRST#
PIN22	5VSB	Power LED	GPIO24/LEDVSB
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	

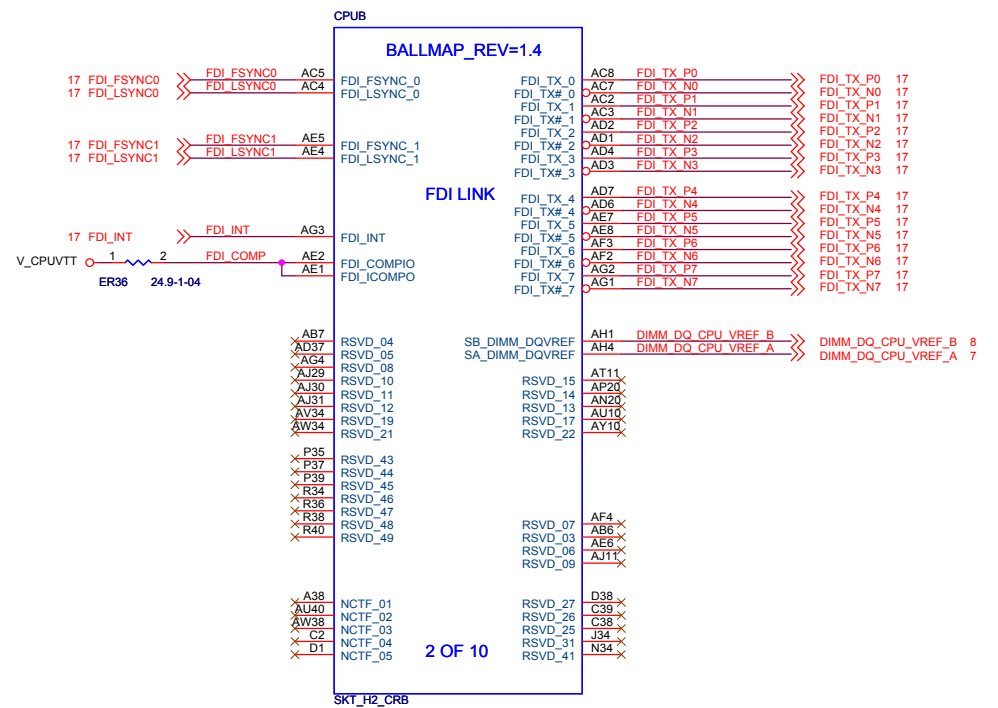


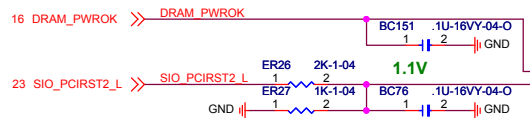
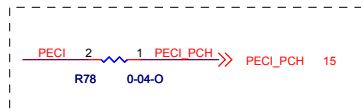
SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
 1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.

1228'10 Jayson :
 Part number modified =

11-018-115124 SOCKET.CPU.LGA 1155P
 SMD..G/F...BLACK.ACA-ZIF-096-P02....
 LEAD-FREE(RoHS/HF).LOTES

20-800-005111 SUBASSY.STEEL....LGA 1155P.....W/BACK
 PLATE.ACA-ZIF-082-P23
LEAD-FREE(RoHS/HF).LOTES



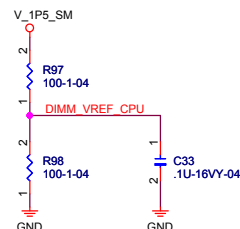


CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG[0..17] HAVE INTERNAL PULL-UPS

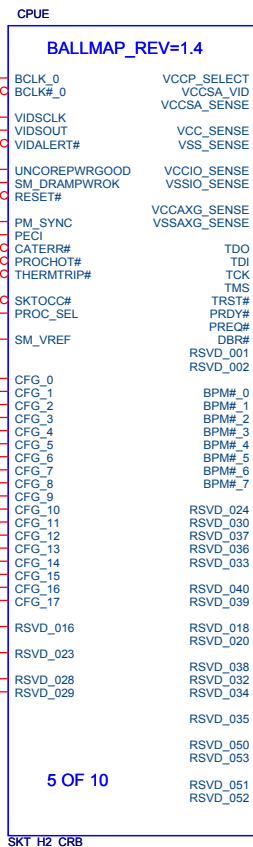
PCIE CONFIG	SELO	SEL1
1 X 16	1	1
2 X 8	0	1

CFG[5:6]:
 01=DEFAULT X16,
 01=2X8,
 10=RESERVED,
 00=X8,X4,X2

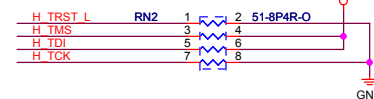


change test point for internal PU Jack05/25

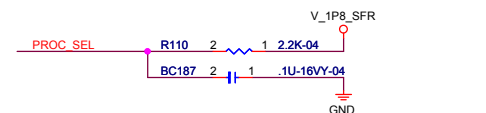
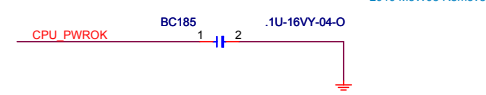
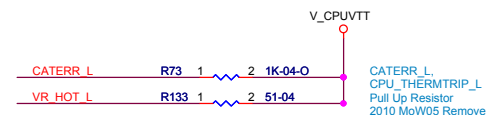
- STP1 1 CFG 0 H36
- STP8 1 CFG 1 J36
- STP16 1 CFG 2 J37
- STP9 1 CFG 3 K36
- STP20 1 CFG 4 L36
- STP25 1 CFG 5 N35
- STP19 1 CFG 6 L37
- STP17 1 CFG 7 M36
- STP21 1 CFG 8 J38
- STP18 1 CFG 9 L35
- STP28 1 CFG 10 M38
- STP30 1 CFG 11 N36
- STP33 1 CFG 12 N38
- STP32 1 CFG 13 N39
- STP34 1 CFG 14 N37
- STP35 1 CFG 15 N40
- STP7 1 CFG 16 G37
- STP2 1 CFG 17 G36



1130*10
 pull high By Jayson Del,
 Pull high on Page11

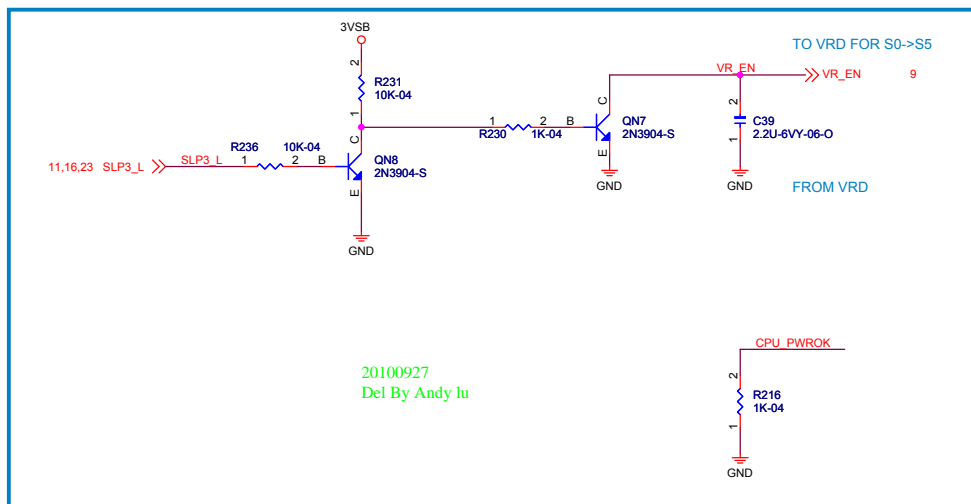


EDS P68/132 has internal PU Jack05/25

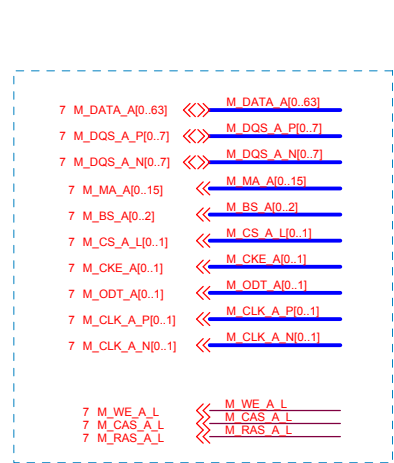


DMI/FDI termination voltage:
 DC coupled: TX/RX to VCC ISF sampled high
 DC coupled: TX/RX to VSS IF sampled low
 AC COUPLED: TX set to VCC/2, RX set to VSS regardless of this strap

Power Down Sequencing Circuit

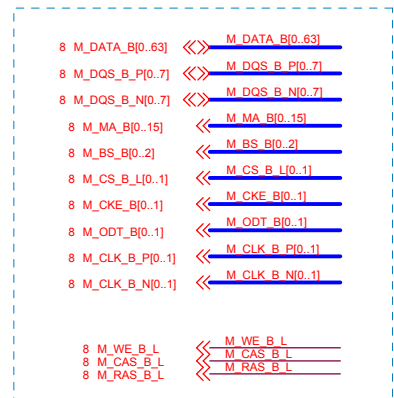


20100927
 Del By Andy lu

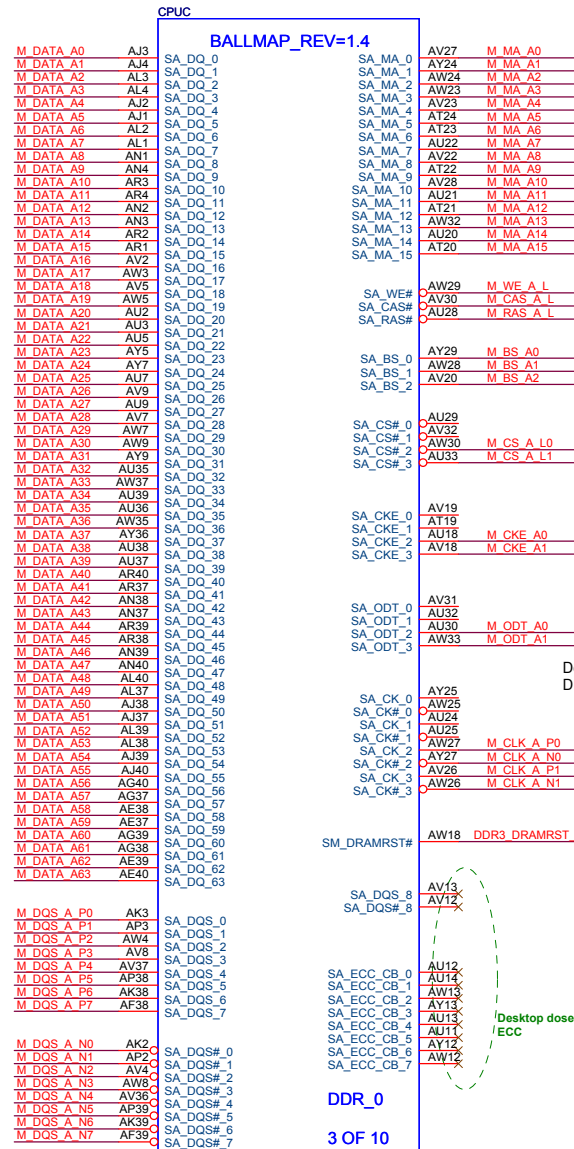


DDR3 CH.A

7,8 DDR3_DRAMRST_L <<> DDR3_DRAMRST_L



DDR3 CH.B



CPUC

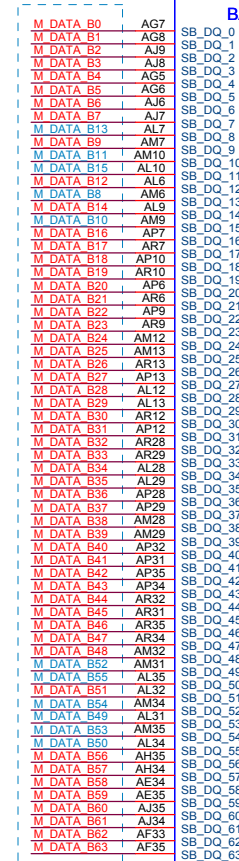
BALLMAP_REV=1.4

DDR_0
3 OF 10

SKT_H2_CRB

DDR3 CH.A

Pay Attention to
This Part!



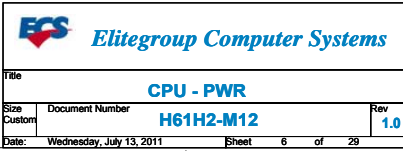
CPUD

BALLMAP_REV=1.4

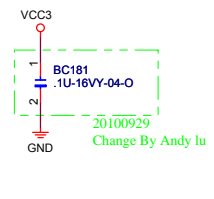
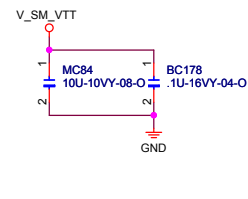
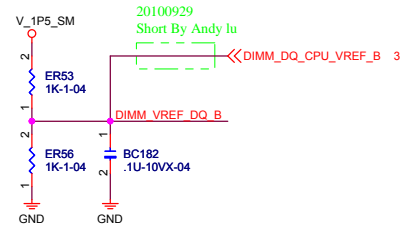
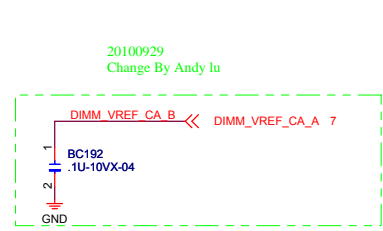
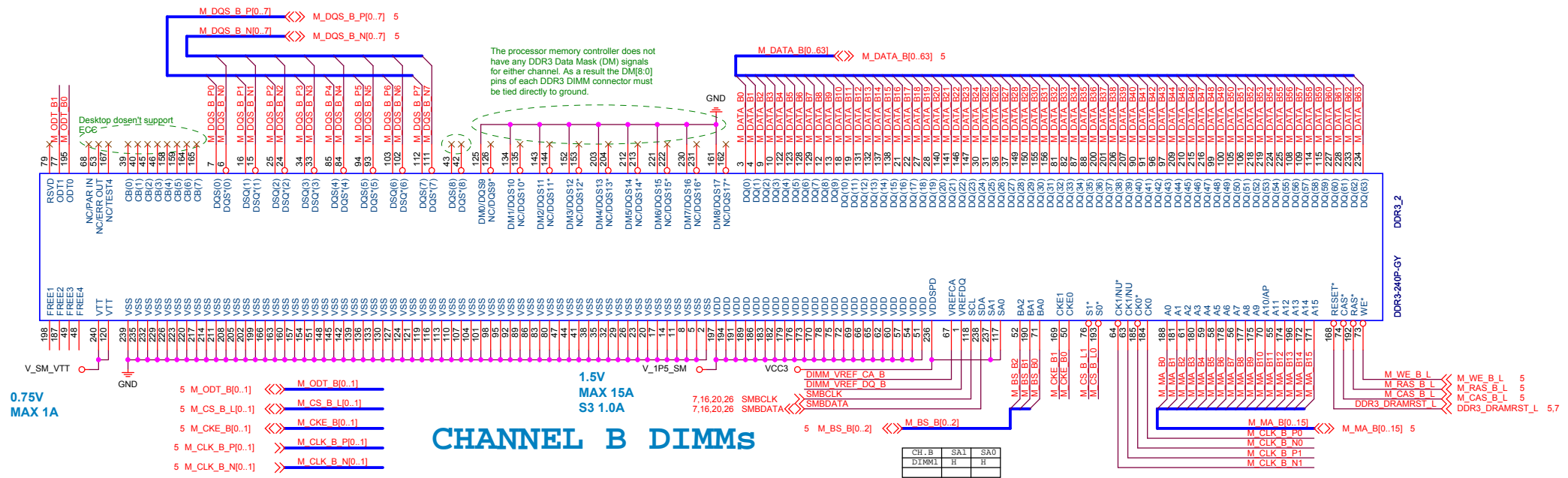
DDR_1
4 OF 10

SKT_H2_CRB

DDR3 CH.B



The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.



Del DIMM3 for always populate DIMM4 first Jack 05/13

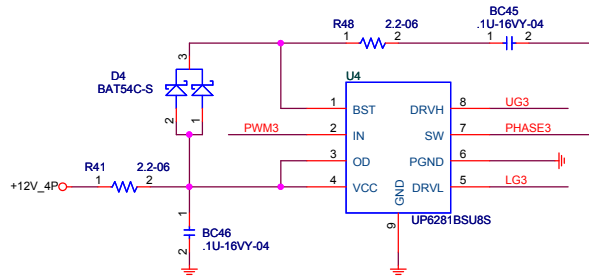
External Connection

VCC
VCORE
VAXG
+12V_4P
VCC3
VIN

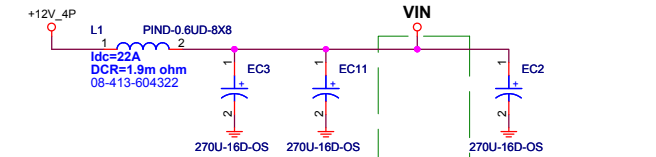
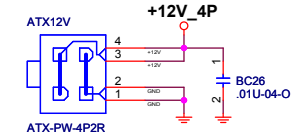
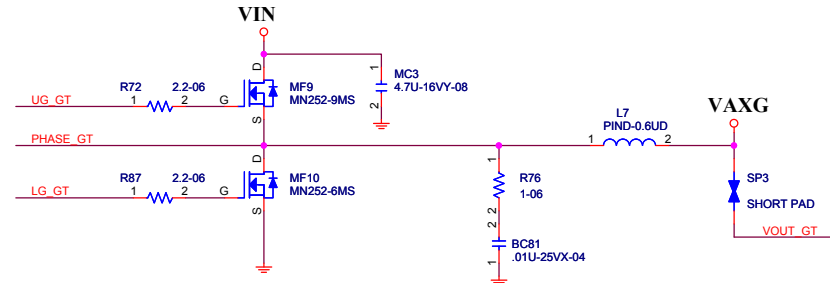
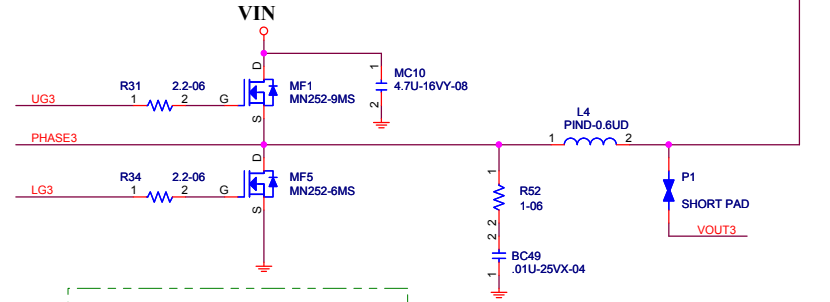
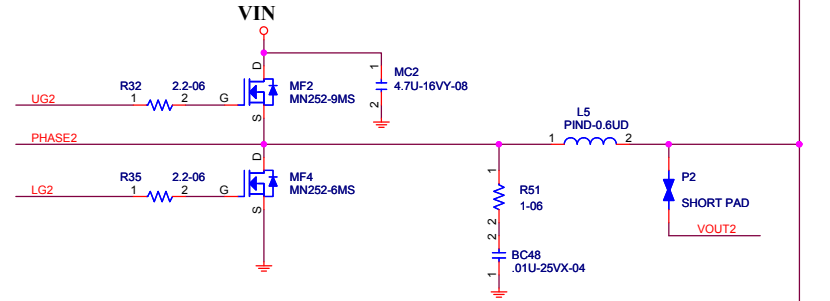
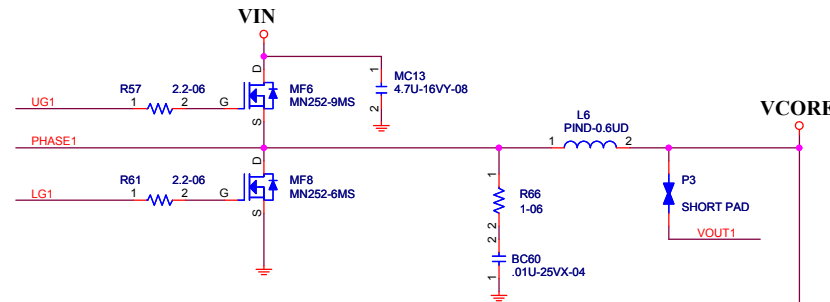
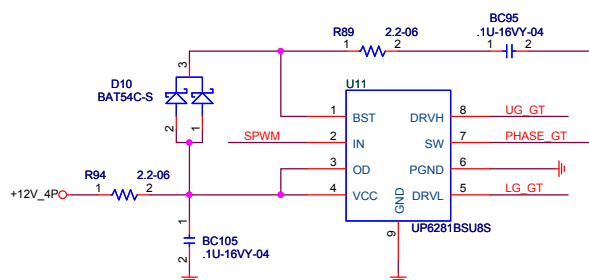
9 UG1
9 LG1
9 UG2
9 LG2
9 PWM3
9 SPWM

9 PHASE1
9 PHASE2
9 PHASE3
9 PHASE_GT

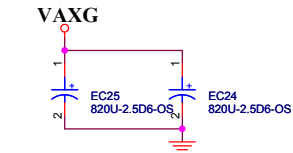
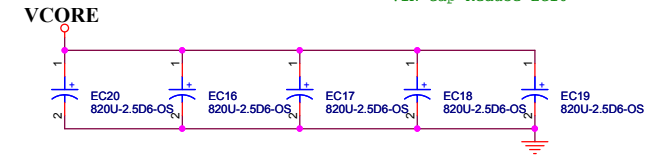
9 VOUT1
9 VOUT2
9 VOUT3
9 VOUT_GT



0504'11 Jayson :
DEL Driver



0504'11 Jayson :
VIN Cap Reduce EC10

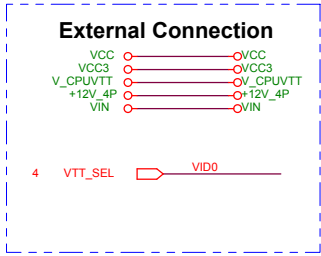
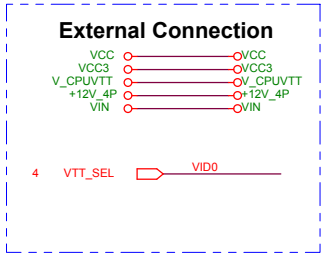
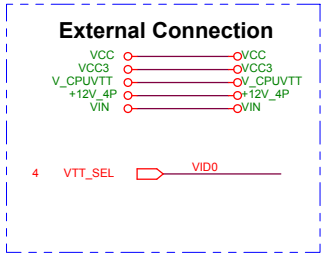


External Connection

VCC3
V_OV_CPUVTT
+12V_4P
VIN

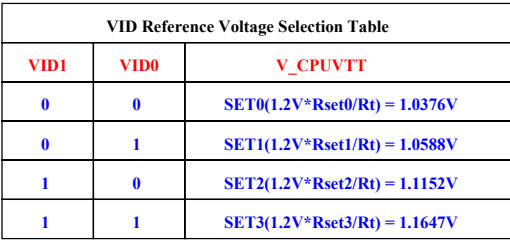
VCC3
VCC3
V_OV_CPUVTT
+12V_4P
VIN

4 VTT_SEL VIDO



VID1	VID0	V _{CPUVTT}
0	0	SET0(1.2V*Rset0/Rt) = 1.0376V
0	1	SET1(1.2V*Rset1/Rt) = 1.0588V
1	0	SET2(1.2V*Rset2/Rt) = 1.1152V
1	1	SET3(1.2V*Rset3/Rt) = 1.1647V

VID1	VID0	V_CPUVTT
0	0	SET0(1.2V*Rset0/Rt) = 1.0376V
0	1	SET1(1.2V*Rset1/Rt) = 1.0588V
1	0	SET2(1.2V*Rset2/Rt) = 1.1152V
1	1	SET3(1.2V*Rset3/Rt) = 1.1647V

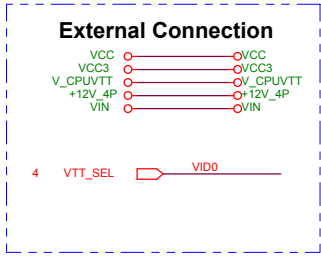
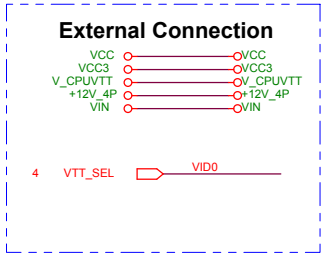


External Connection

VCC3
V_OV_CPUVTT
+12V_4P
VIN

VCC3
VCC3
V_OV_CPUVTT
+12V_4P
VIN

4 VTT_SEL VIDO



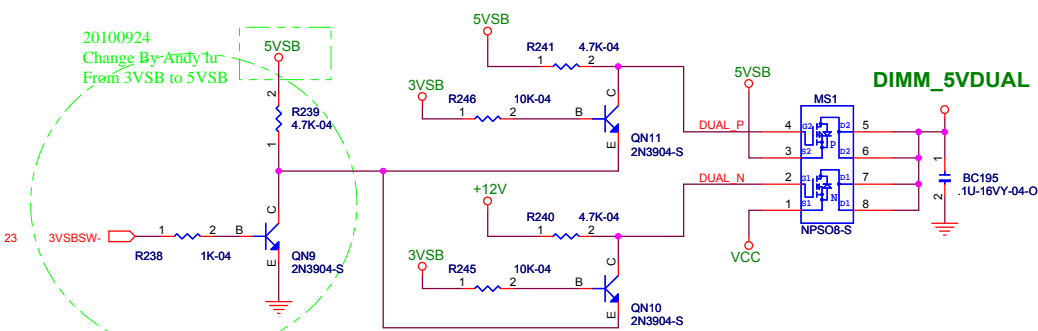
External Connection

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V_OV_CPUVTT
+12V_4P
VIN

VCC3
VCC3
V_OV_CPUVTT
+12V_4P
VIN

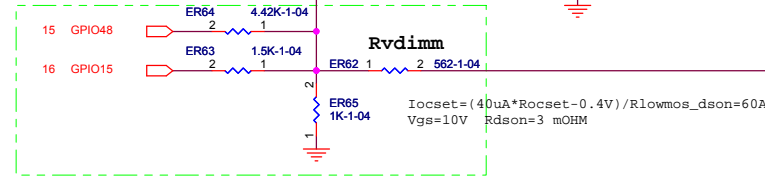
4 VTT_SEL VIDO

20100924
Change By Andy lu
From 3VSB to 5VSB

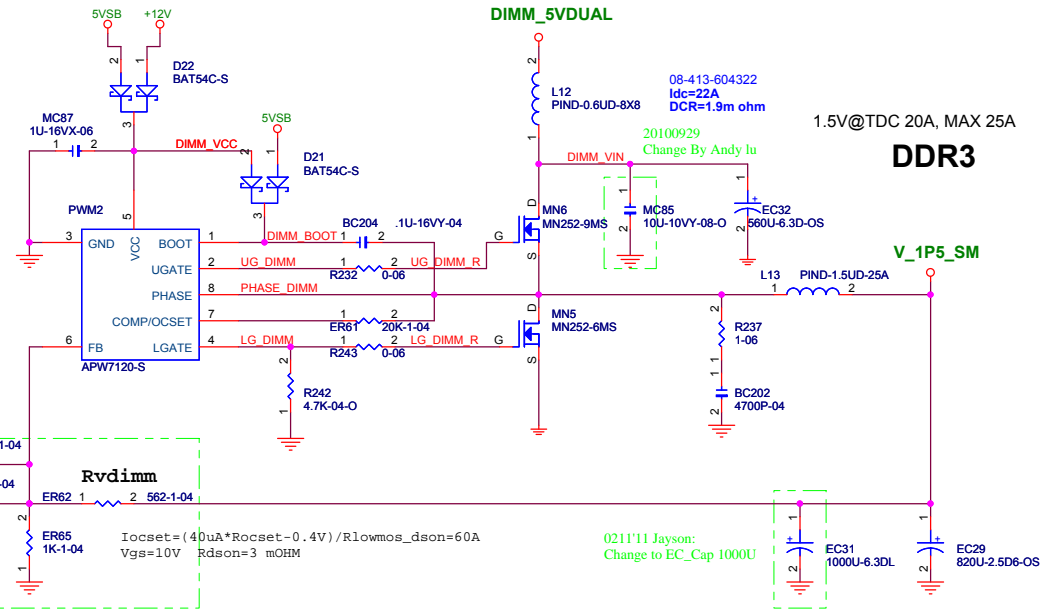


DIMM_5VDUAL

1207'10 Jayson :
Add By Jayson
for Down Voltage of DIMM



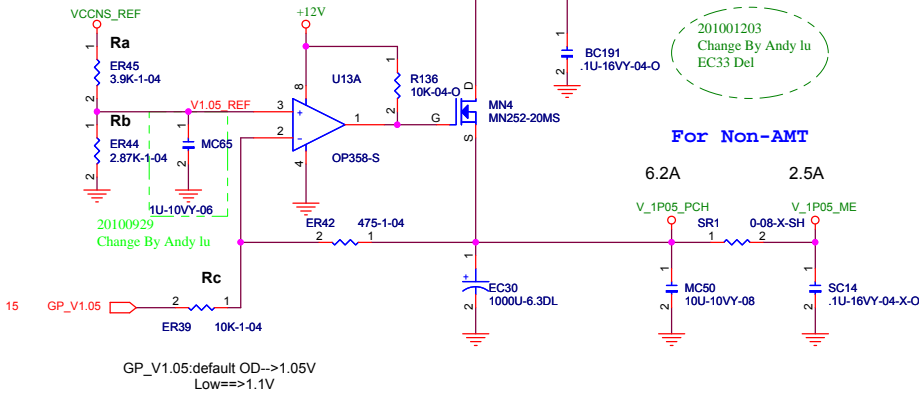
DIMM_5VDUAL



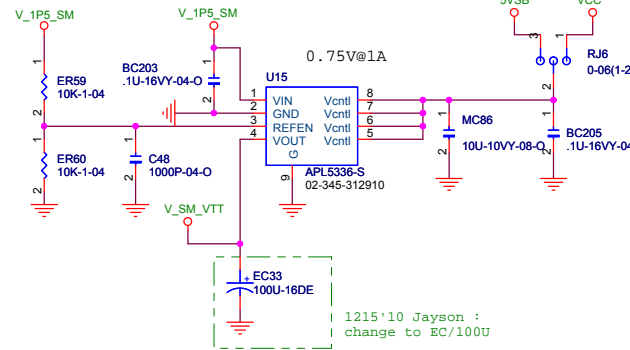
DDR3

1.5V@TDC 20A, MAX 25A

reserve for LG_DIMM refer to VCC Jack 06/22



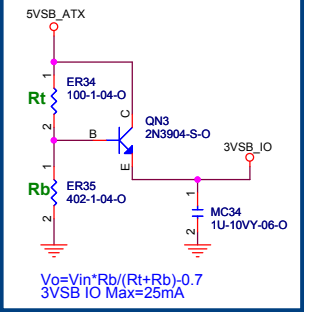
For Non-AMT



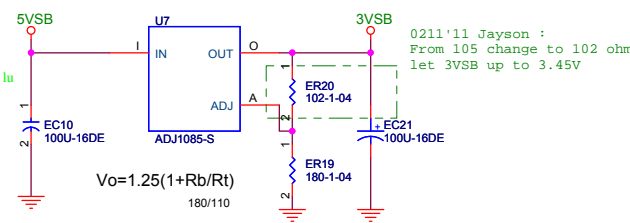
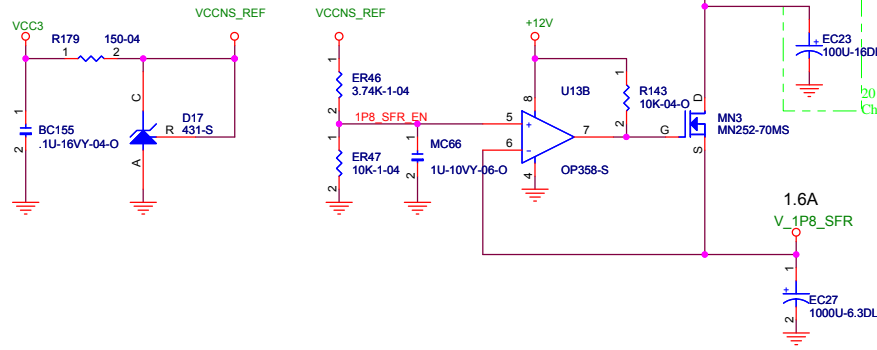
Refer to page28

Sd

3VSB_IO



1210'10 Jayson :
3VSB_IO 先線路預留不上
;SIO有內轉power.



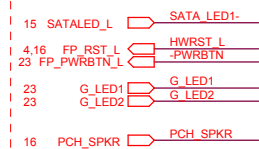
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USB3.0 W/O S3 ADJ1086-S 02-347-086760 (SOT-223)



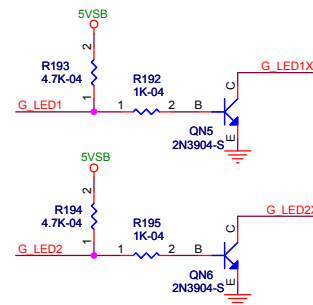
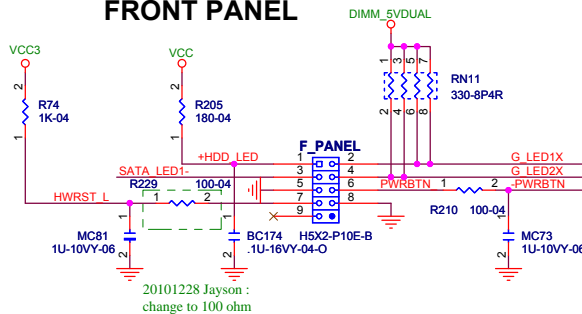
Elitegroup Computer Systems

Title		DC/DC VDIMM/DDR_VTT/5VDUAL	
Size	Document Number	H61H2-M12	
Custom		Rev 1.0	
Date:	Wednesday, July 13, 2011	Sheet	12 of 29

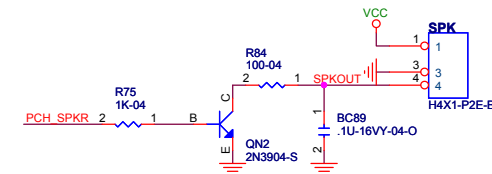
External Connection



FRONT PANEL

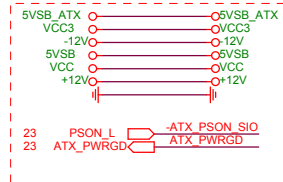


	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
G	GB	YB	OFF	OFF	OFF

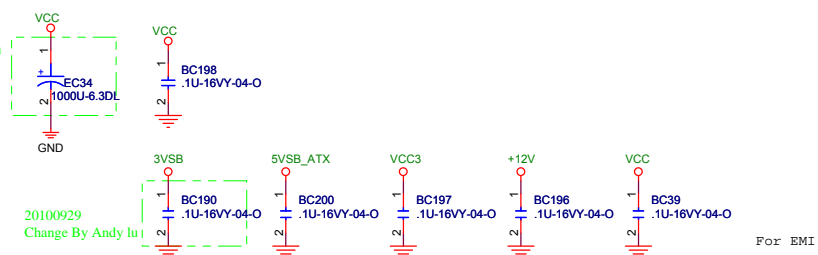
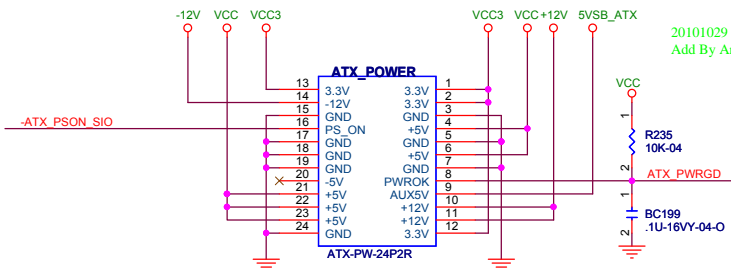


POWER CONNECTOR

External Connection

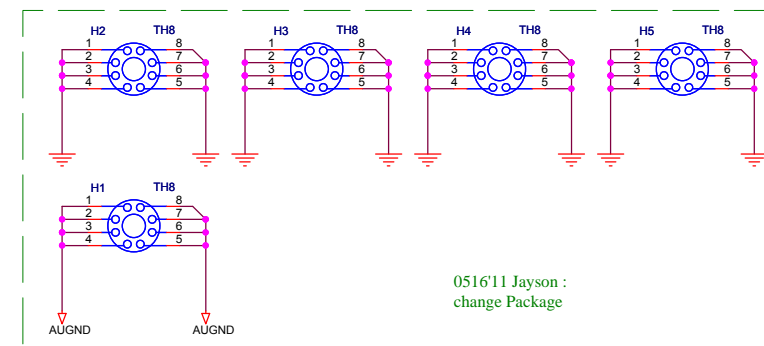
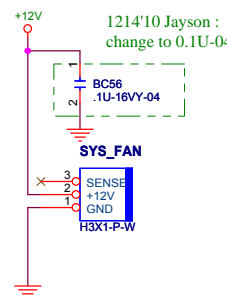
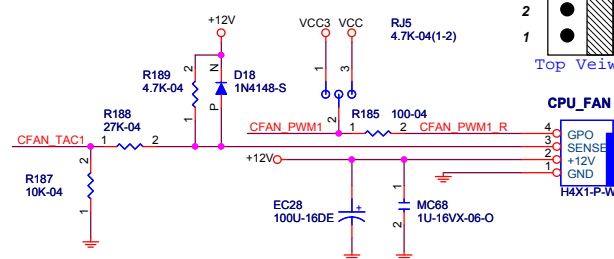
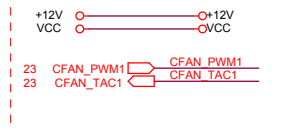


F_PANEL		
1	2	+HDD_LED
3	4	
5	6	PWR
7	8	
9		

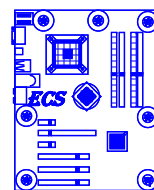


FAN

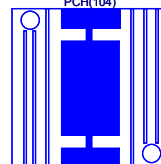
External Connection



PCB



PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM



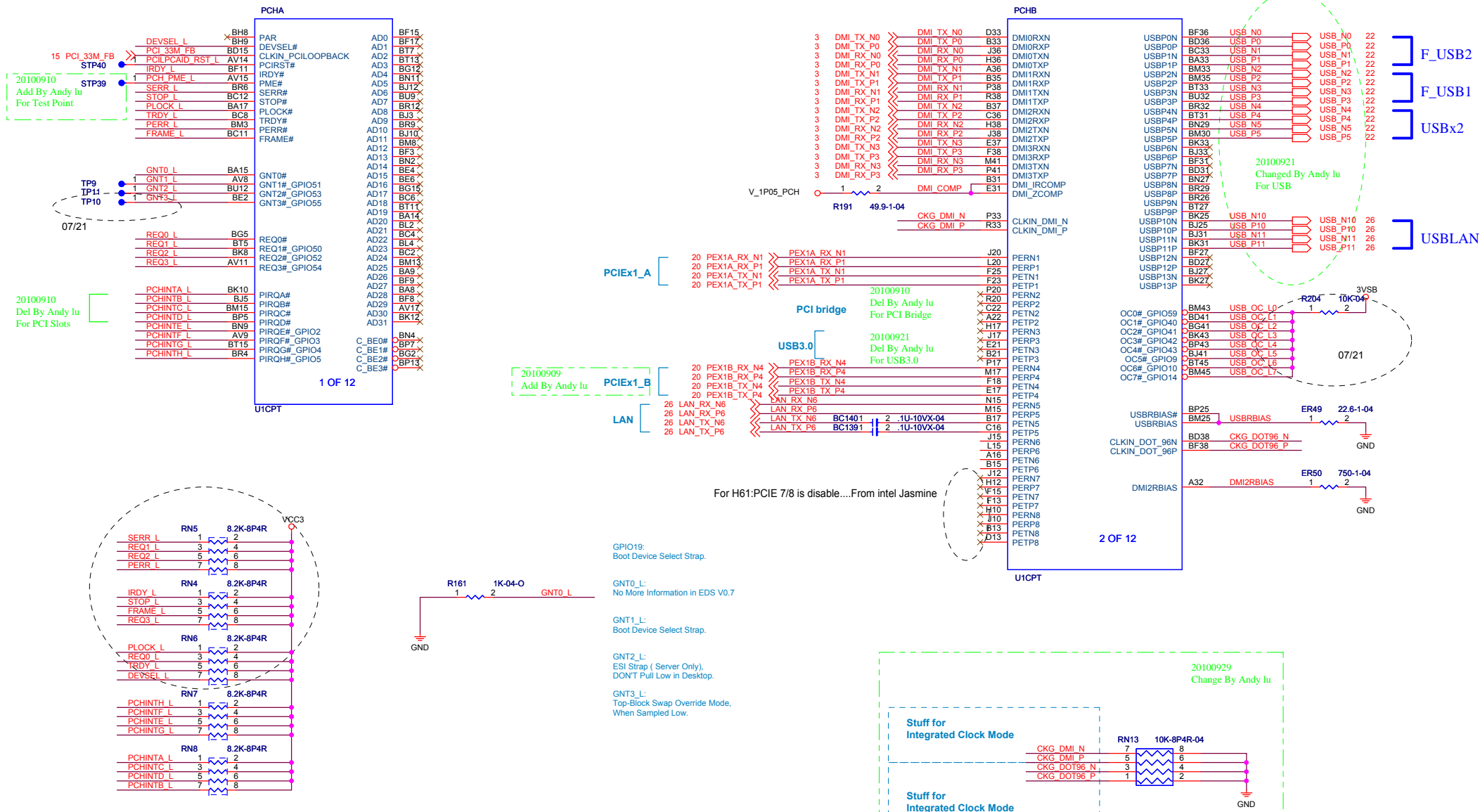
20-120-012242
5series PN:20-120-010851

0214'11 Jayson :
PCH Heat Sink change to smaller.



Title	
Front Panel,FAN,PowerConn,GND,104	
Size	Document Number
Custom	H61H2-M12
Date:	Wednesday, July 13, 2011
Sheet	13 of 29
Rev	1.0

For H61:USB Port 6/7/12/13 is disabled....From 440377 file

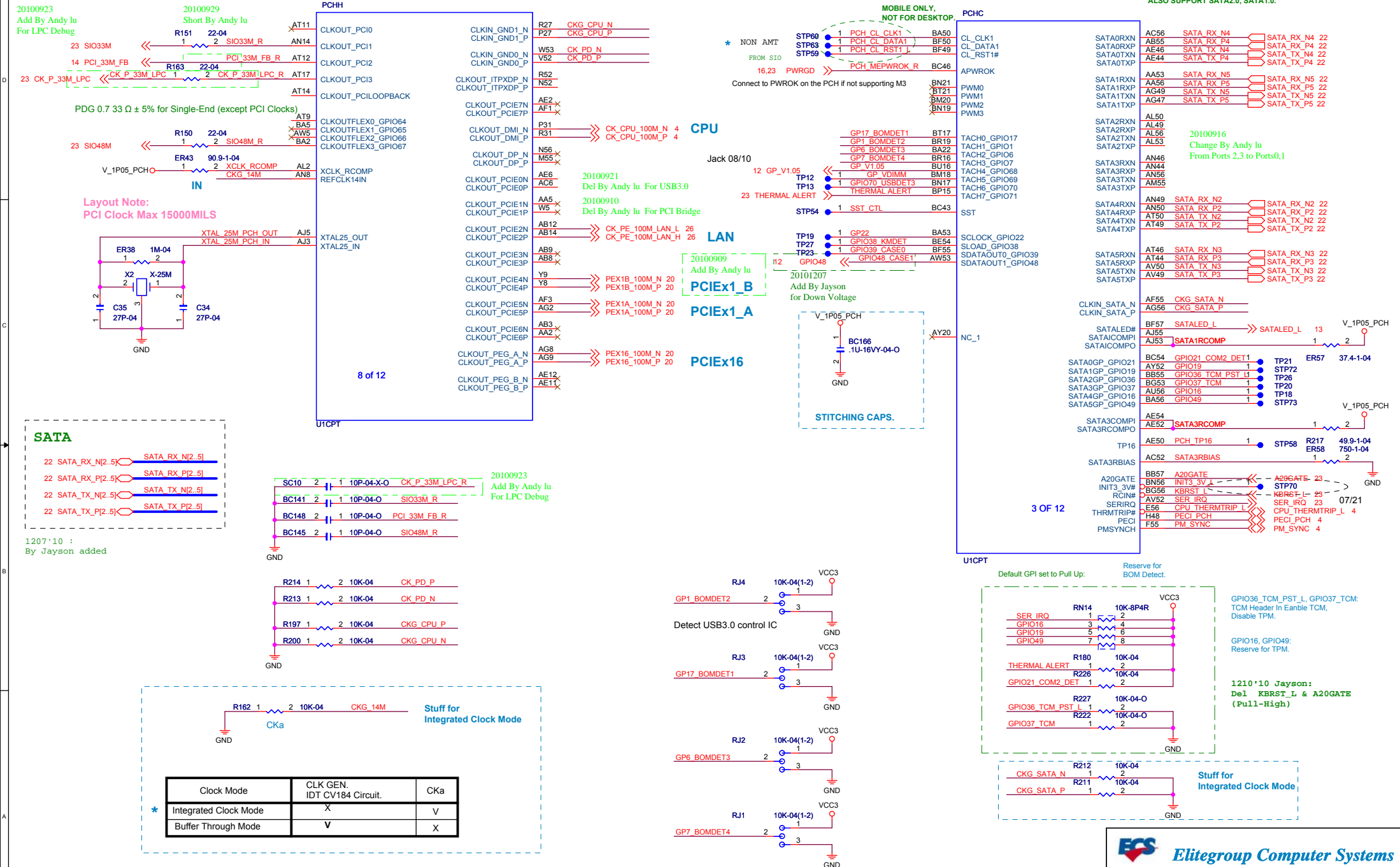


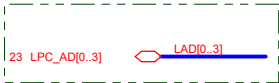
GNT[0..3]#
GPIO19
have been internal pull high to +VCC3

Boot Device Select:

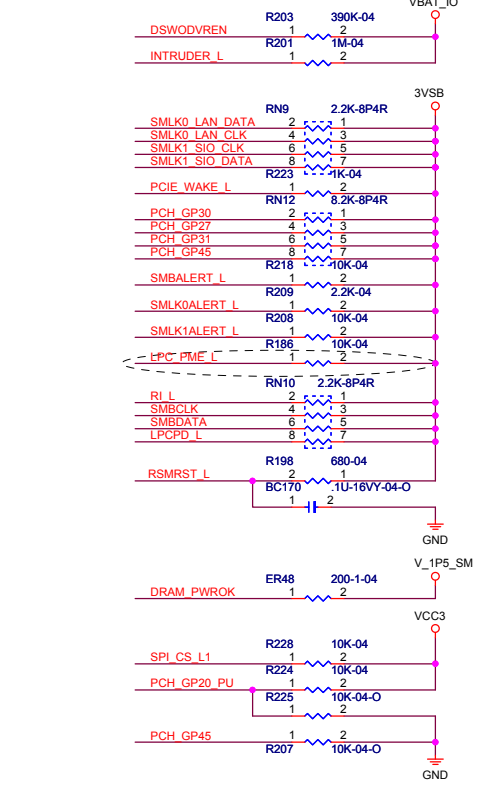
BOOT_DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

For H61:SATA port2/3 is disable....From 440377 file
ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0,
ALSO SUPPORT SATA2.0, SATA1.0.

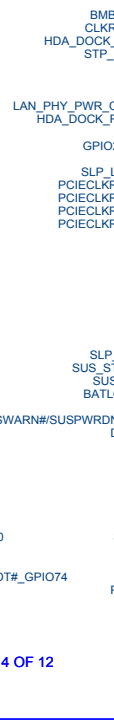
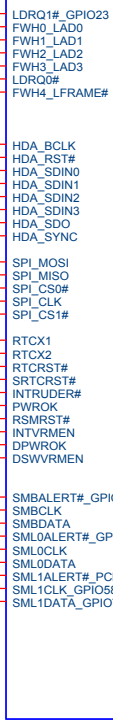




1207'10 :
By Jayson added

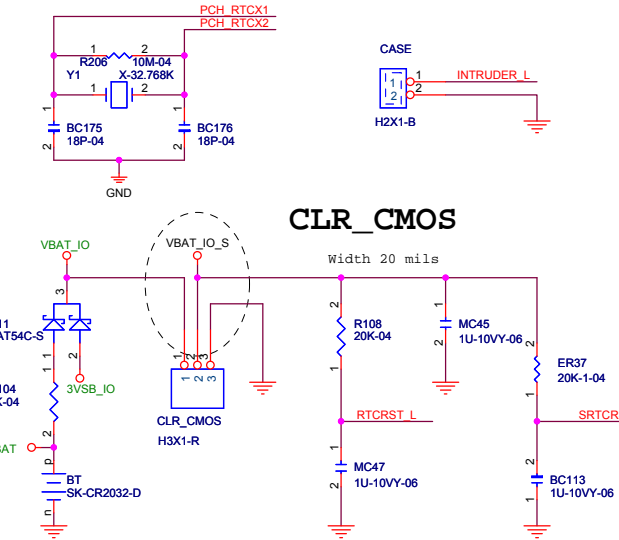


PCHD



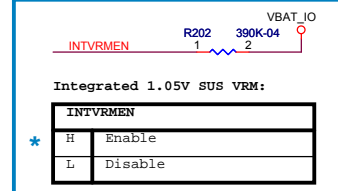
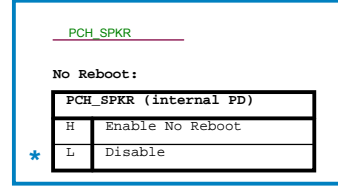
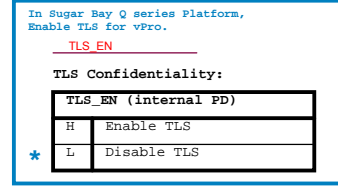
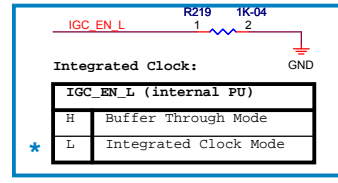
4 OF 12

U1CPT

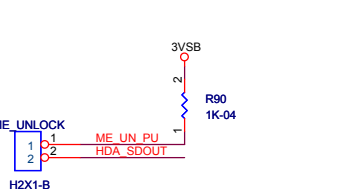
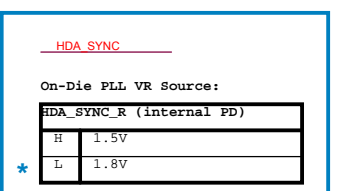
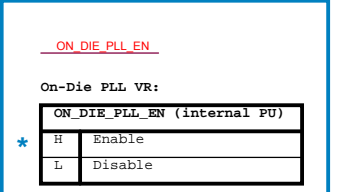
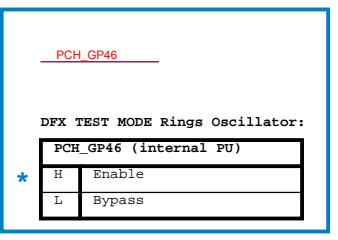
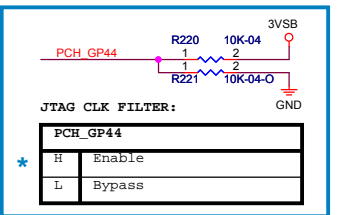
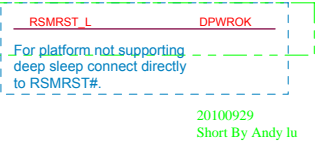


CLR_CMOS

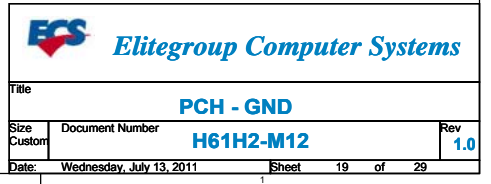
Buffer Through Mode / Integrated Clock Mode have been changed to F/W Strap.
Default: Integrated Clock Mode
Doc. Cougar Point Platform Controller Hub (PCH) Family EDS Update V0.7.1



When Deep Sleep not implemented:
1.PCH_GP30, PCH_GP27 need to be Pull Up.
2.VCC0SDW3_3 should to be connected to +3VSB.
3.SLP_SUS_L, SUSACK_L left unconnected.
4.SUSWARN_L may be used as GPIO30.(Reference to 1.)



ME Enable/Disable	
ME_UNLOCK	
1-2	UNLOCK
Float	LOCK




```
0504'11 Jayson :  
DEL DVI
```

```
0504'11 Jayson :  
DEL DVI
```

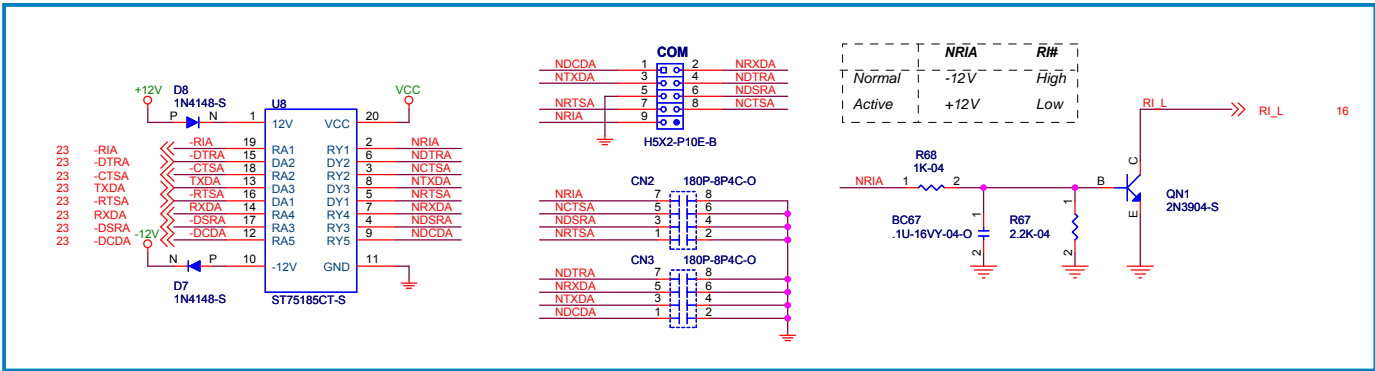
```
0504'11 Jayson :  
DEL DVI Connector
```

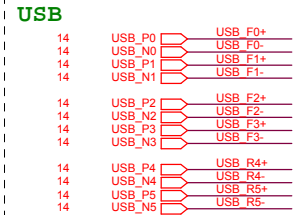
```
0504'11 Jayson :  
DEL DVI
```

0504'11 Jayson :
DEL Fuse & Diode

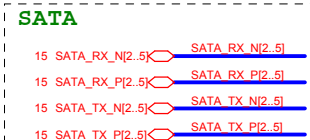
0504'11 Jayson :
DEL DVI

```
1202'10 Jayson :  
Del HDMI
```

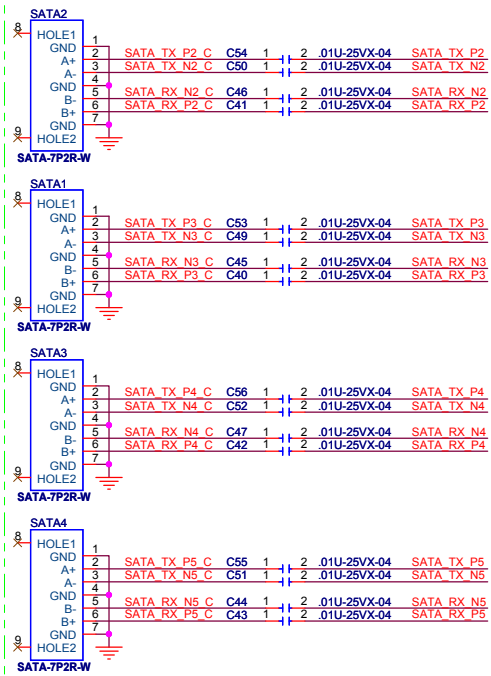




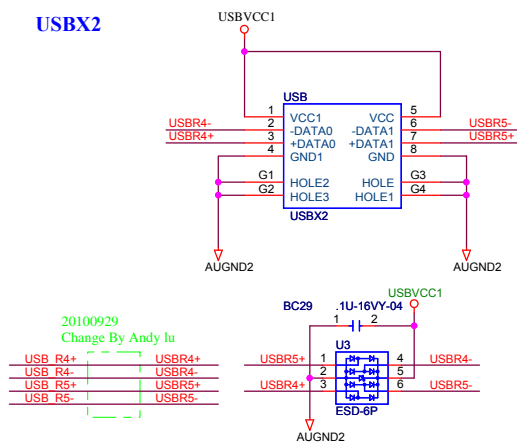
0504'11 Jayson :
DEL SLP_S3_N



Layout Note:
SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%

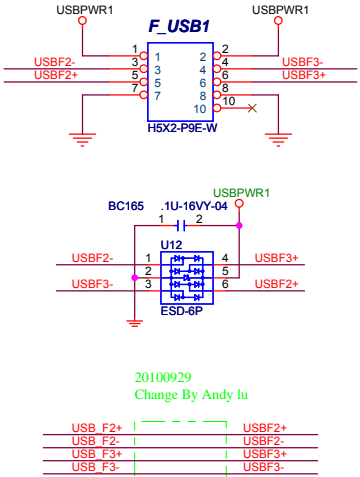


USBX2



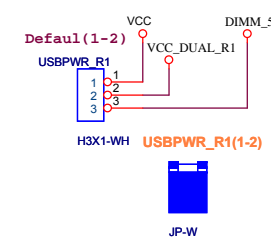
0504'11 Jayson :
From USBPWR2 change to USBPWR1

F_USB1



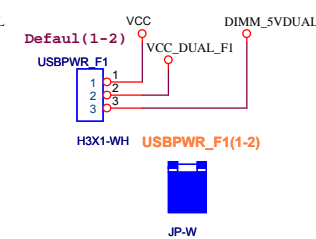
USBPWR_F / R	
1-2	VCC *
2-3	DIMM_5VDUAL

USB x2 & PS/2 & USBLAN

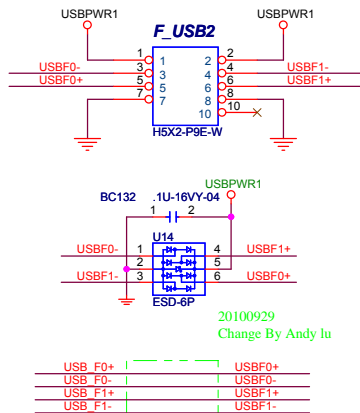


0504'11 Jayson :
ADD Jumper.

F_USB1&2

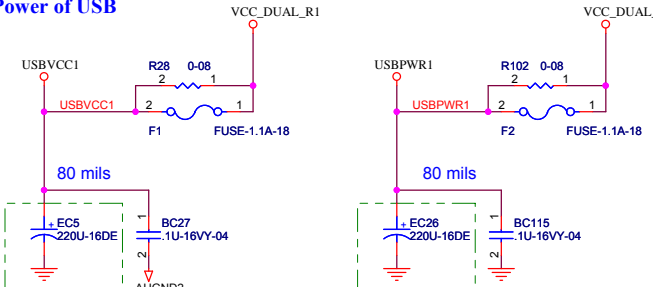


F_USB2



0504'11 Jayson :
From SW_Power change to Jumper.

Power of USB

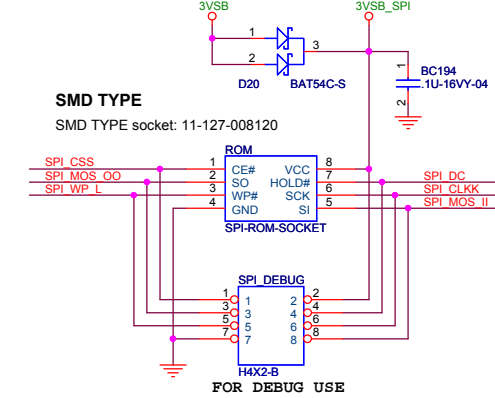


1228'10 Jayson :
EC1,EC4 From 100U change to 220U.

0504'11 Jayson :
EC28 From 100U change to 220U.

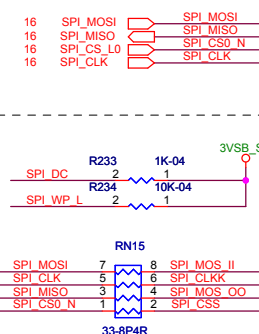
0504'11 Jayson :
From SW_Power change to Jumper.

SPI

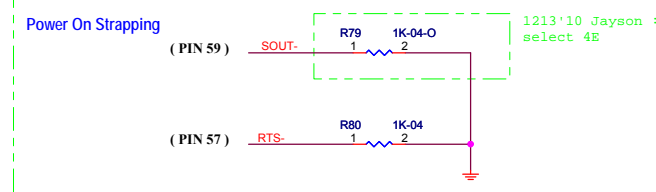
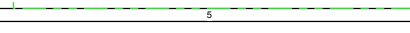
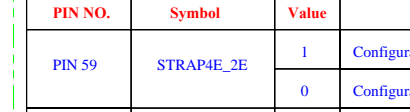
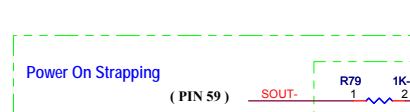
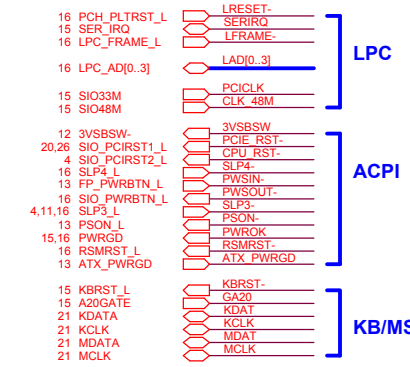
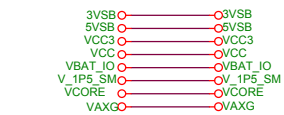


若上SMD SPI ROM, MP or A5後不上ROM Socket.

SPI



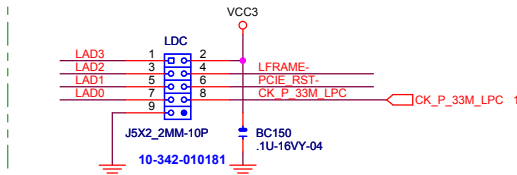
External Connection



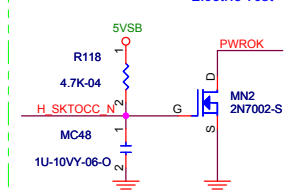
PIN NO.	Symbol	Value	Description
PIN 59	STRAP4E_2E	1	Configuration Register I/O port is 4E/4F.(Default)
		0	Configuration Register I/O port is 2E/2F.
PIN 57	STRAP_PWOK	1	PWOK(pin 35) for AMD(Default)
		0	PWOK(pin 35) for Intel

1231'10 Jayson : LDC take the place of TPM.

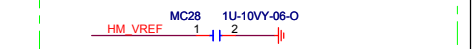
LPC DEBUG HEADER



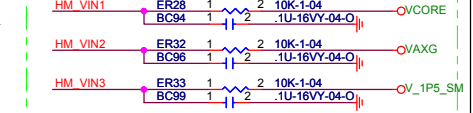
Electric Test



Thermal Sensing



Voltage Sensing



BIOS SELECTION

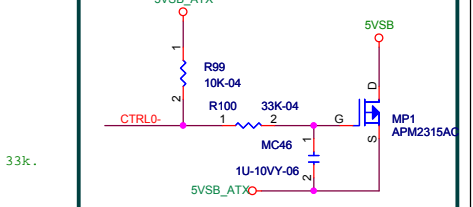


EUP

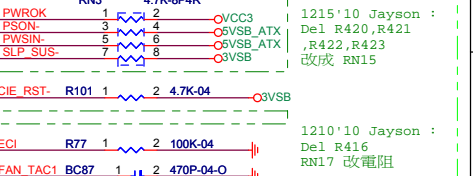
	W/O EUP	W EUP
Sb	V	X
Sc	X	V
Sd	X	V

page 12

Sc



Pull high & Pull low



Elitegroup Computer Systems

Title: **SIO-F71808A**

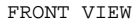
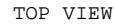
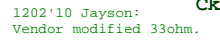
Size Custom: Document Number: **H61H2-M12**

Date: Wednesday, July 13, 2011 Sheet 23 of 29

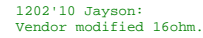
Rev: **1.0**

16 FP_AUD_DETECT << HDPANEL_DETECT

Non re-tasking for rear panel



FRONT - AUDIO



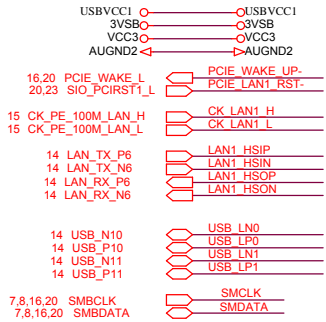
```
1203'10 Jayson: Del SPDIF-OUT
```



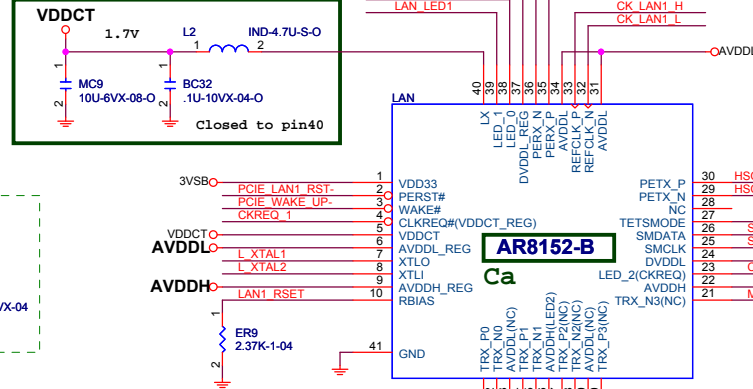
Size Custom	Document Number H61H2-M12	Rev 1.0
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Date:	Wednesday, July 13, 2011	Sheet	25	of	29
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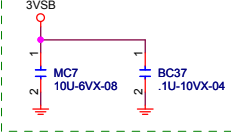
External Connection



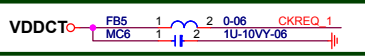
Ca



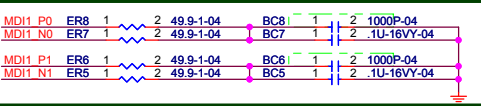
Closed To Pin1



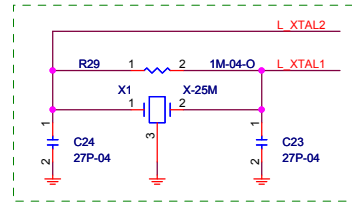
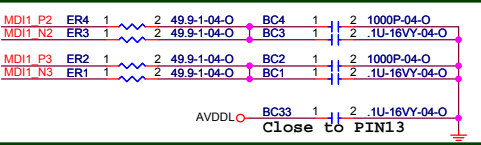
Ch



Ci



Cg

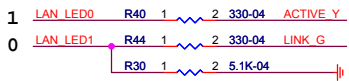


BOM Difference

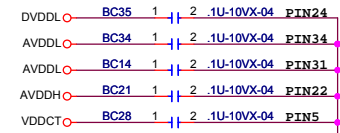
	AR8151-B 1000M	AR8152-B 10/100M	AR8161-B 1000M
Ca	AR8151-B	AR8152-B	AR8161-B
Ch	V	X	X
Cc	USBX2-LAN-1000	USBX2-LAN-100	USBX2-LAN-1000
Cd	X	V	X
Ce	0-04	.01U-25VX-04	0-04
Cf	V	X	V
Cg	V	X	X
Ch	X	V	X
Ci	V	V	X
Cj	V	X	V
Ck	V	X	X
Cl	X	X	V
Cm	V	V	X
Cn	V	V	X

HW Strapping

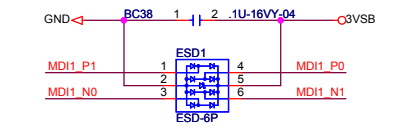
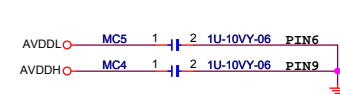
LED0 : 0 -> OC disable
1 -> OC enable
LED1 : 0 -> VDDCT_REG enable
1 -> VDDCT_REG disable



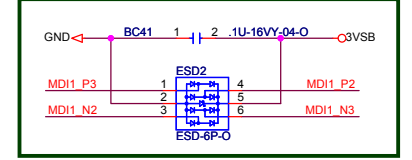
Closed To PWR Loading Pin



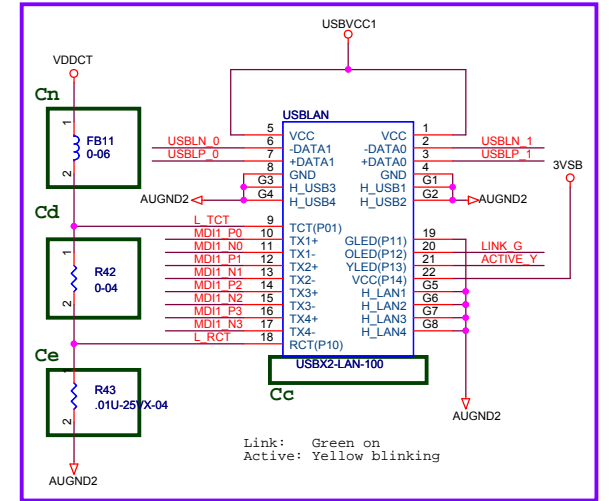
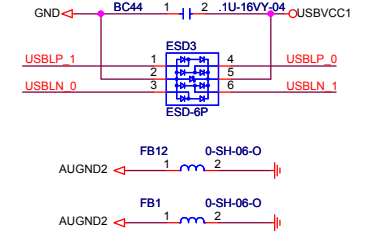
Closed To PWR Source Pin

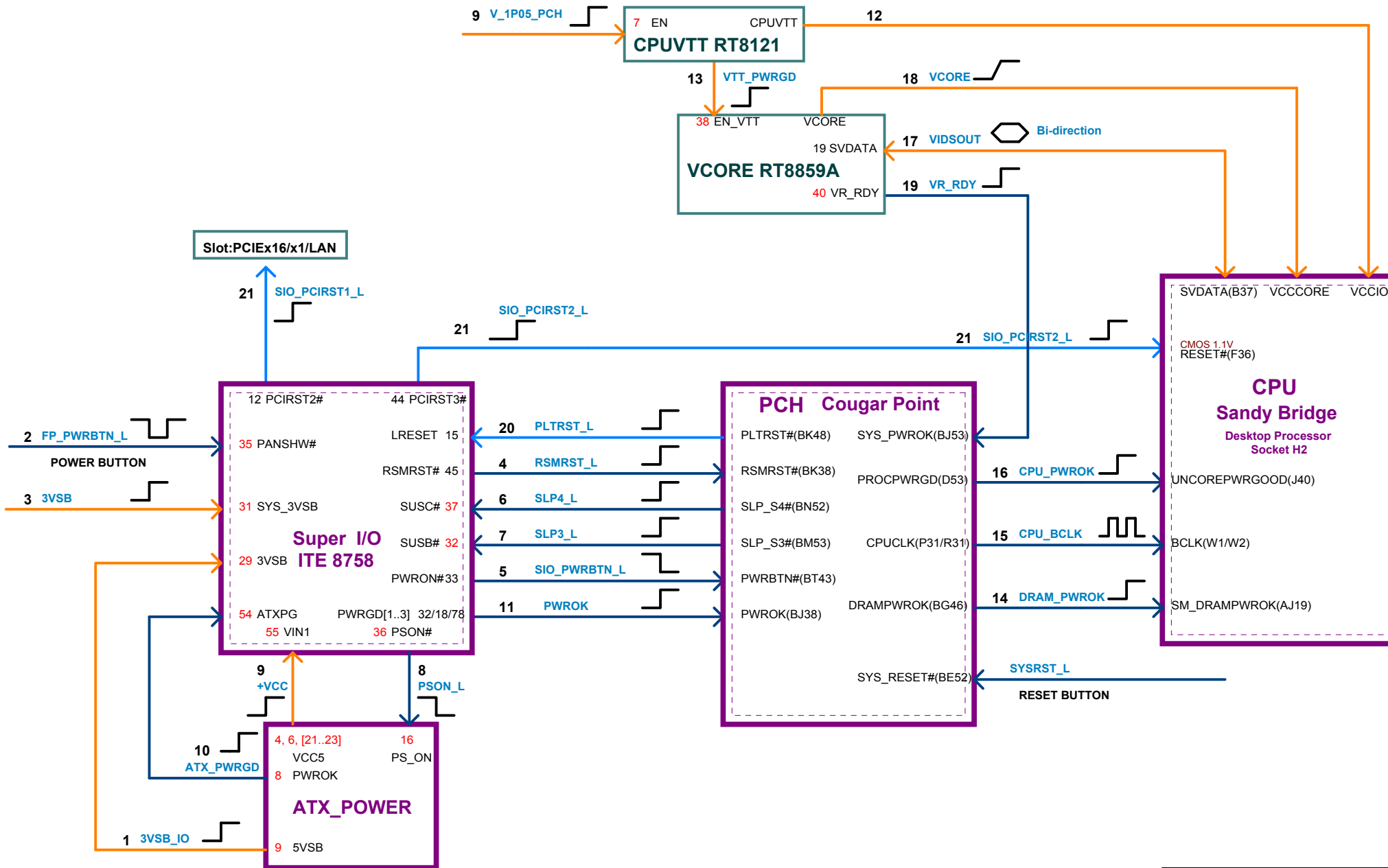


Cf



20100929
Short By Andy lu





NOTE:
Sugar Bay Platform has two clock mode:
1.Integrated Clock Mode (Generate by PCH)
2.Buffer Through Mode (Generate by Clock Gen.)
If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.
Please refer to
Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD
Page.13 PCH - SATA, SATA CONN for CLK IN PD
Page.14 PCH - MISC, F/W Strap
Page.15 PCH - CLK IO, CKG - CV184 for Option

1129'10 By Jayson Del CK505

1129'10 By Jayson modified

